

FIG. 1  
(PRIOR ART)

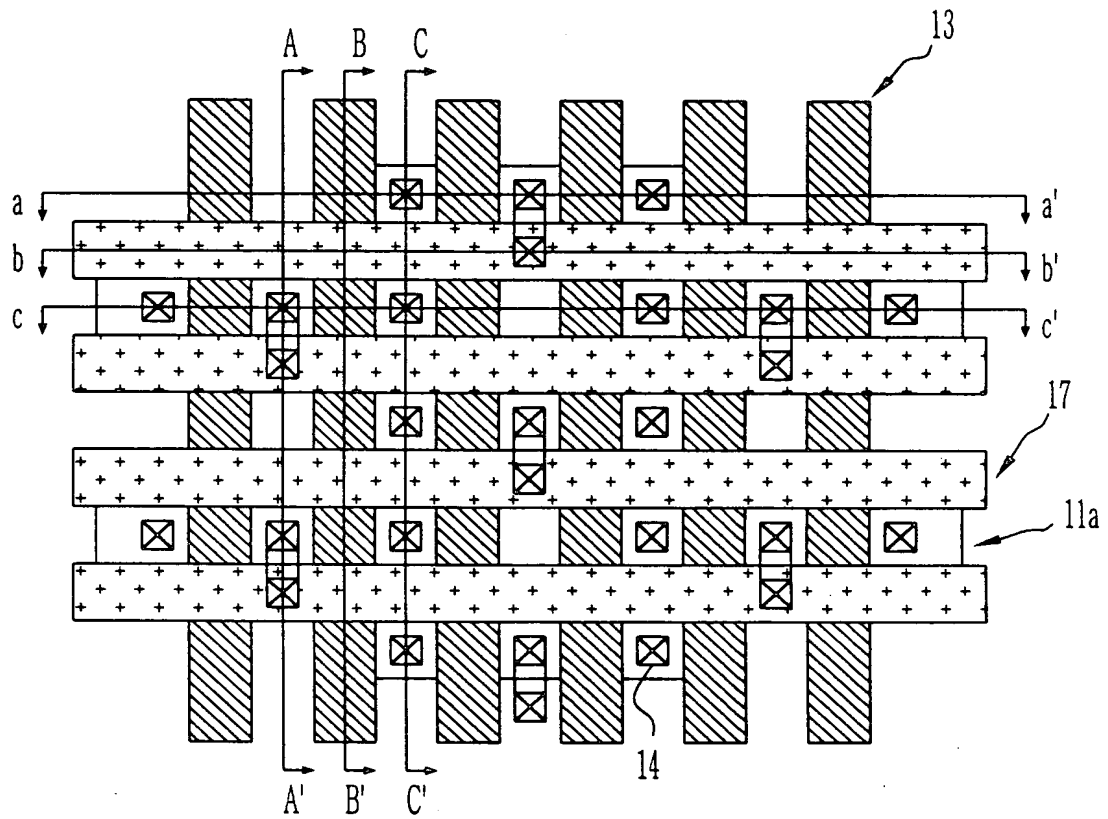


FIG. 2A  
(PRIOR ART)

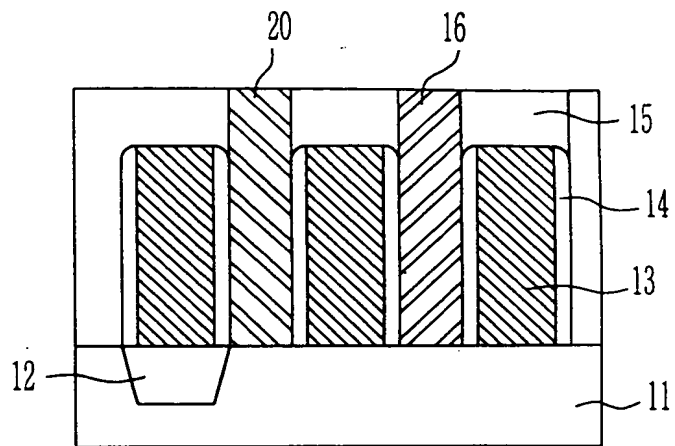


FIG. 2B  
(PRIOR ART)

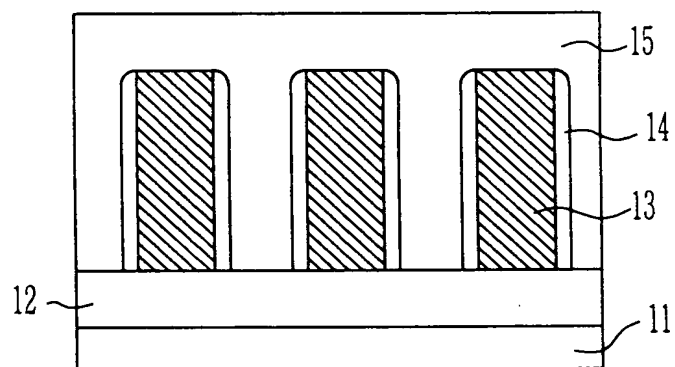


FIG. 2C  
(PRIOR ART)

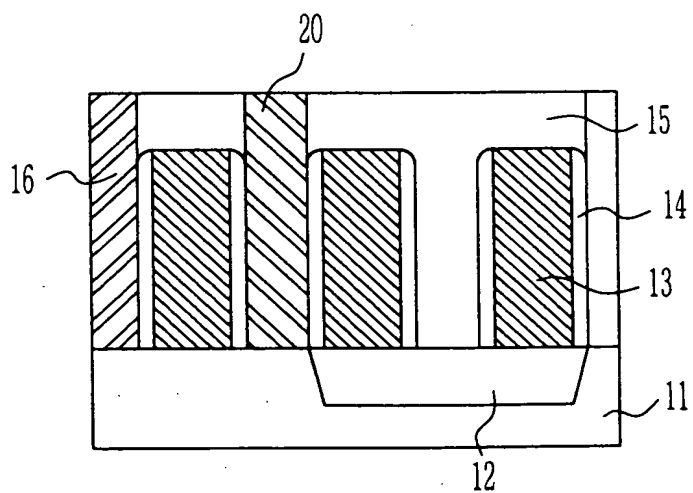


FIG. 3A  
(PRIOR ART)

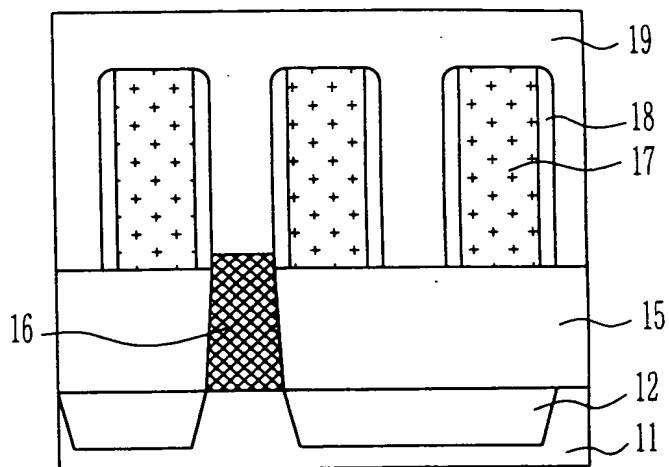


FIG. 3B  
(PRIOR ART)

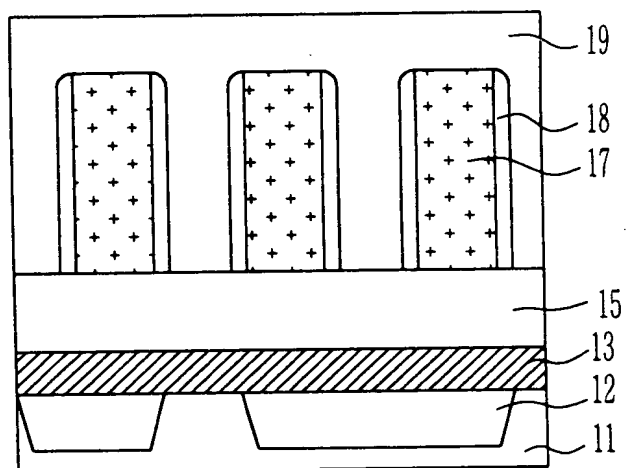
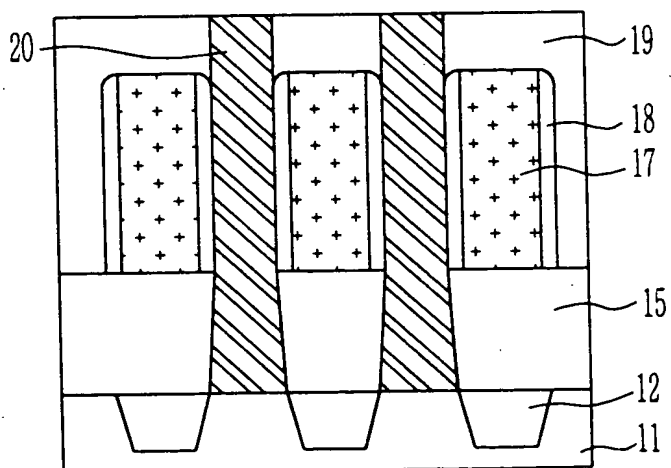


FIG. 3C  
(PRIOR ART)



A cross-sectional view of a semiconductor device. The device consists of a substrate 11 with three trapezoidal pillars 12. A layer 13 is formed on top of the pillars 12. A layer 15 is formed on top of the layer 13. Three vertical pillars 17 are formed on top of the layer 15. Each pillar 17 contains a pattern of '+' signs. The pillars 17 are separated by a gap 18. The width of the gap 18 is labeled W. The width of the pillars 17 is labeled W'. The length of the pillars 17 is labeled L.

FIG. 5A

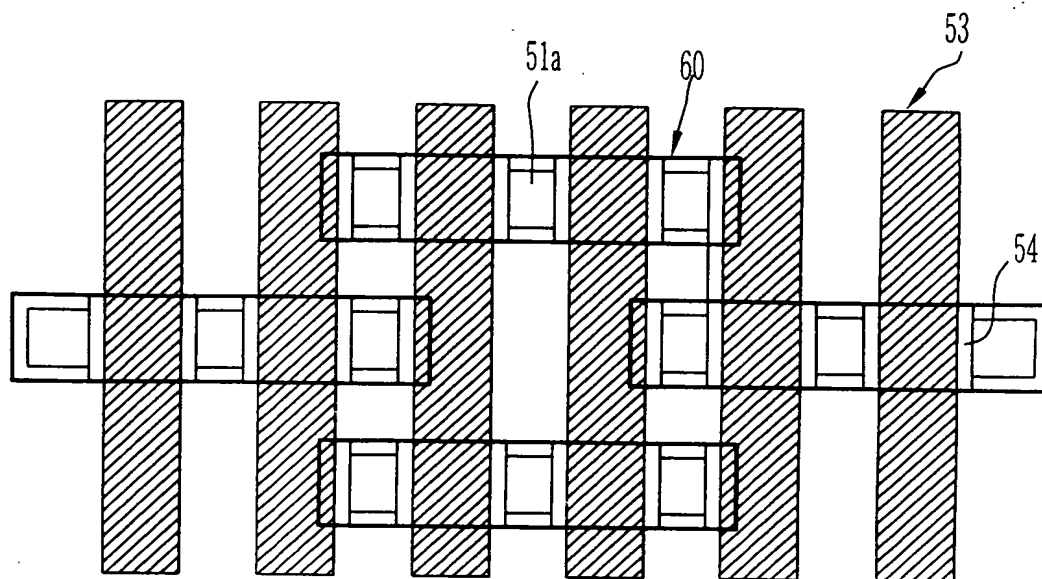


FIG. 5B

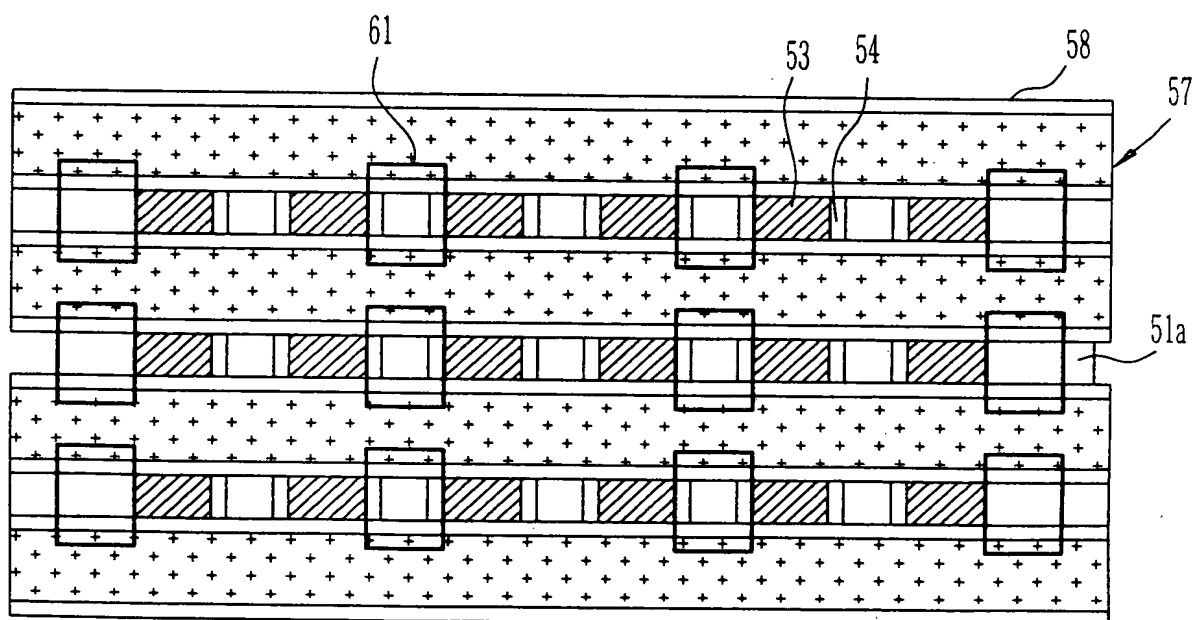


FIG. 6A

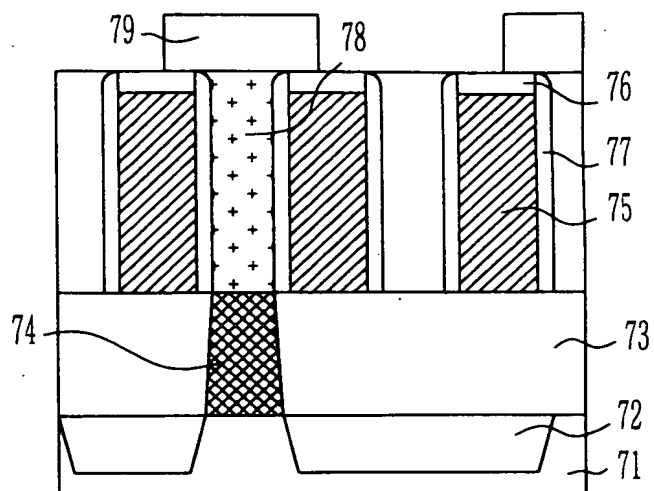


FIG. 6B

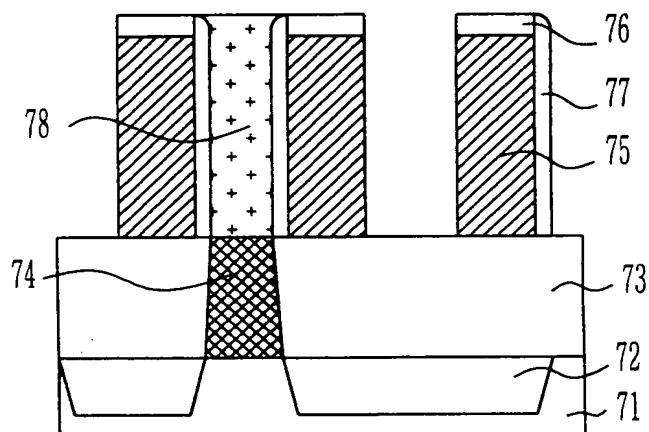


FIG. 6C

